New System Large Scale Integration for Elevator Drive Control

Shigeki Yamakawa, Hiroshi Gokan, Hiroshi Araki, Hiroyuki Ikejima
Mitsubishi Electric Corporation Inazawa Works, Japan and
Mitsubishi Electric Corporation Design Systems Engineering Center, Japan

ABSTRACT

Mitsubishi has developed a new System-LSI chip incorporating a majority of the elements of our elevator control system. The previous control system included an original digital signal processing CPU core for the inverter/converter control, PWM controller, Car-speed limiting CPU core, and other car-control logic circuits. All of these components have been integrated on this one LSI-chip with approximately 250,000 logic gates. This integration has realized minimization of the control unit, high reliability, improvement of the control performance, and a reduction in cost.

1. Background of Development

The drive control system for Mitsubishi's previous generation of high-speed elevators is shown in Figure1. The Car Control CPU manages the control sequencing and car movement. A Drive Control CPU manages current control of the converter/inverter using a fully digital PWM technique. A Digital Signal Processor adjusts the current command in response to the current feedback loop.

In the development of the latest system using a system LSI design, the following design goals were identified to realize minimization of the control unit, improvement of the control performance, and cost reduction, all at the same time.

(1) Provide high-speed current control calculation to eliminate peripheral circuitry. Specifically the Td (Inverter Dead Time) compensation circuit which improves the current distortion at the ZERO crossing point.

(2) Combine the high-speed current control calculation circuit and other functional circuits for car control (e.g. Encoder counters, digital PWM circuit., Safety logic etc.) into a single unit capable of being realized on a single LSI Application Specific Integrated Circuit.

2. Key Points of Development

The new System LSI specialized for elevator control has been named the AML(Associated Management Logic) chip. Through its development, the following points were addressed and solved in order to realize this new design.

(1) Realization of high speed current control calculation circuit

(2) Design / Verification method for large scale logic circuit including processor cores

(3) Concurrent design of hardware and software to minimize the development period

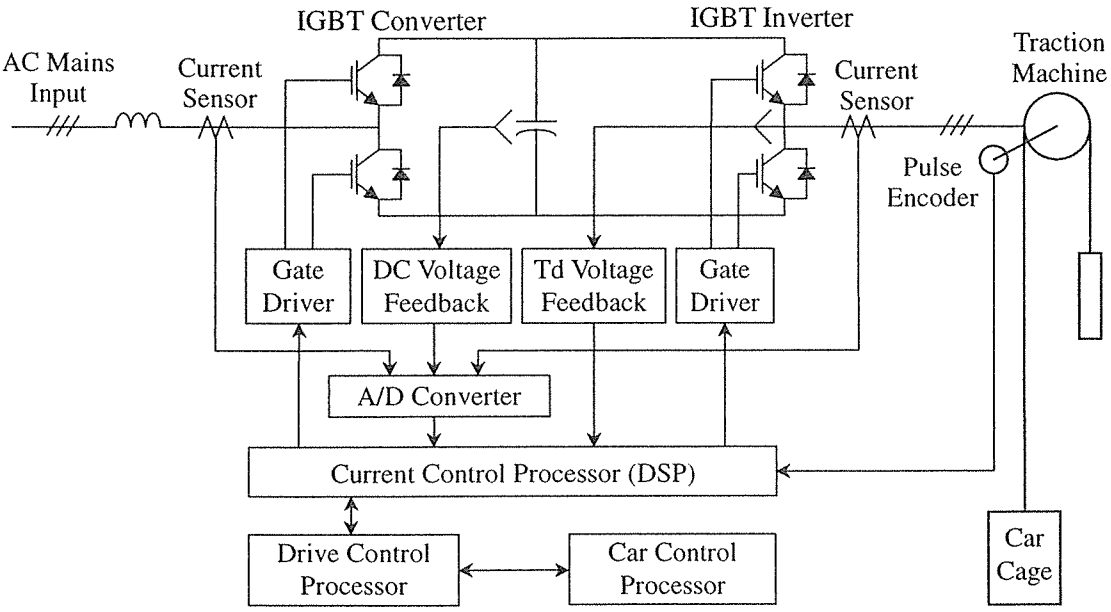


Figure 1. Configuration of High-Speed Elevator Control System

3. Configuration of AML Chip

3.1 System Outline

Figure 2 shows the block diagram of the AML chip. Most of the required logic circuits for car control and motor driving are integrated on this single chip, so that only the Car Control(CC) CPU, flash memories, and serial transmission logic are needed as external devices. Each functional block is described below:

-MCP(Motor Control Processor) is an original data processing core which calculates and controls the converter/inverter current in a short processing cycle.

-PWM(Pulse Width Modulation) units and the Encoder Counting Unit for speed feedback are connected to MCP bus-line.

-32bit CC-CPU is provided as a host CPU via Dual Port Memories which are connected to both the MCP bus-line and CC bus-line. The Encoder Counting Unit is also connected to the CC-CPU for the calculation of the car position.

-8bit Speed Limiting CPU is provided independently from other logic to observe the car speed. Data transmission between CC-CPU and SL-CPU are performed through an asynchronous Register File with hand shaking. Safety hard-wired logic circuit is connected to both the CC-CPU bus-line and SL-CPU bus-line.

-Specification of the AML chip is shown in Table 1.

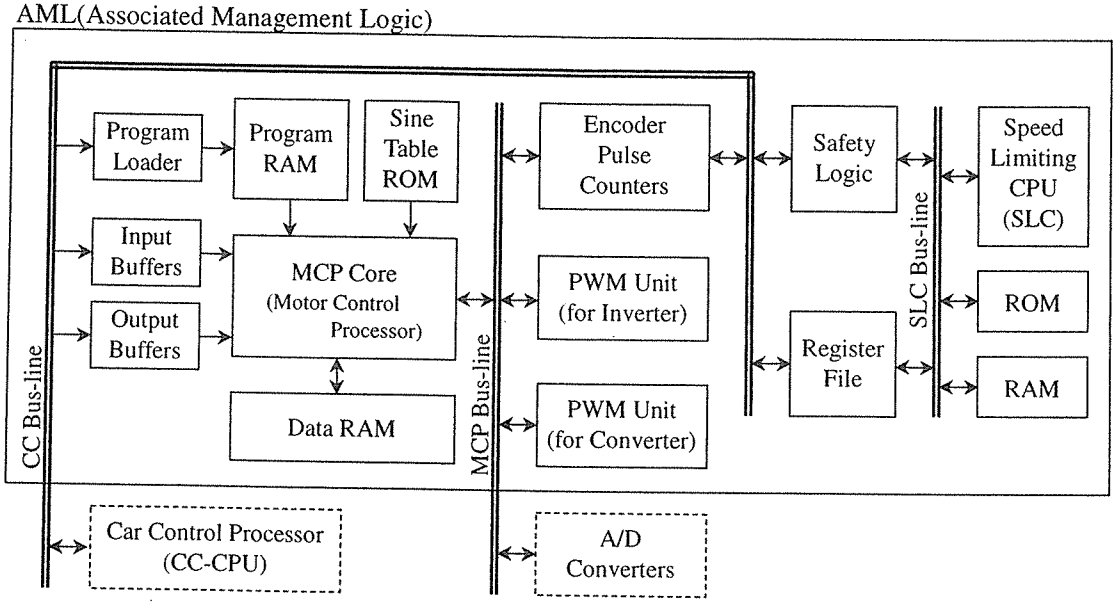


Figure 2. Configuration of AML Chip

Design Rule	0.5μm Cell-Based IC
Package	240pin Fine-Pitch QFP Plastic Package
Supply Voltage	3.3V
Operating Frequency	40MHz
Included Logic	User Logic : 100kG (Including MCP Core) General Processor Core : 12kG (for SLC) Synchronous SRAM : 8kB Synchronous Dual Port SRAM : 2kB ROM : 4kB

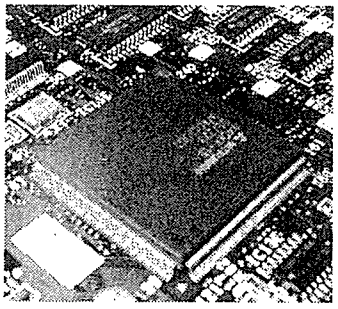


Table 1. Specification of AML Chip

3.2 Motor Control Processor

3.2.1 Performance Requirement

Due to the characteristics of digital control, the higher the frequency of the current control, the more precisely the output current and motor speed can be controlled. The previous control system made use of external circuitry to clean up the discontinuities of the zero crossing of the output waveform inherent with inverters. This new generation control system does not make use of such external circuitry. So it was necessary to increase the operating frequency in order to smooth out the inverter output reducing the influence of Td(6μs has been employed for IGBT inverters). Figures 3.1 through 3.4 show the relationship between crossover angular frequency of current control and car acceleration in an actual high speed elevator.

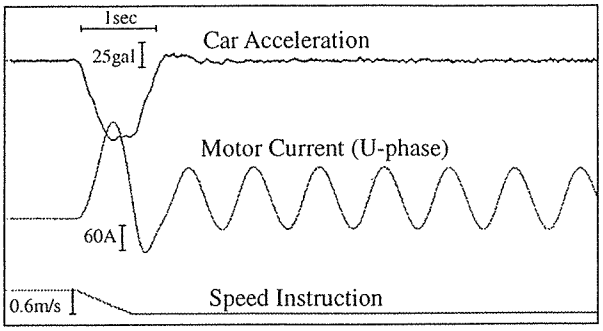


Fig3.1 ω_c=500rad/s, with Td Compensation

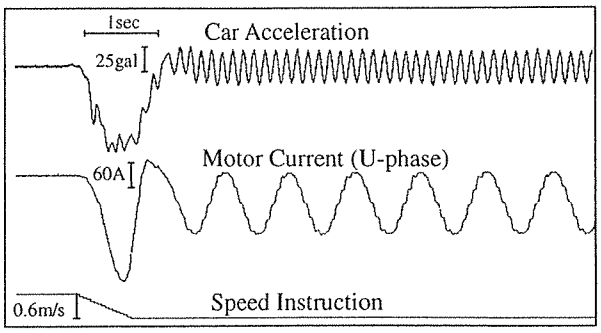


Fig3.2 ω_c=500rad/s, without Td Compensation

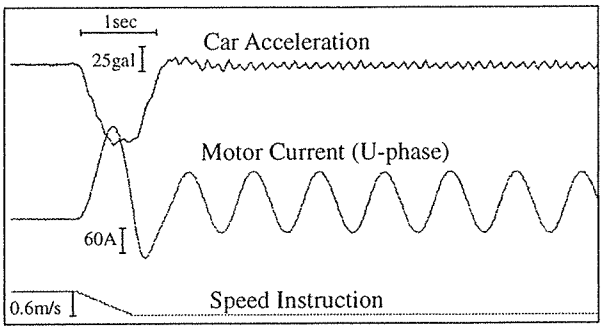


Fig3.3 ω_c=2000rad/s, without Td Compensation

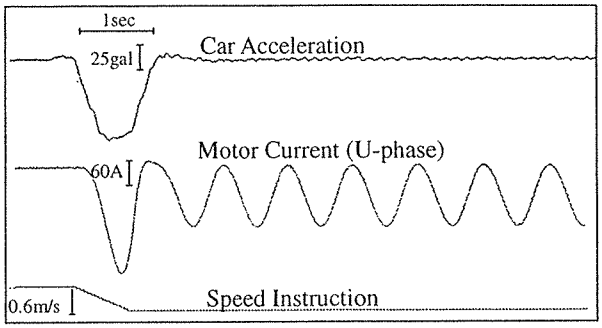


Fig3.4 ω_c=5000rad/s, without Td Compensation

Fig3 Relationship between Crossover Angular Frequency ω_c and Car Acceleration (Td-6μs, in Balanced Load)

(1) Figure3.1: Crossover Angular Frequency ω_c = 500rad/s, with H/W Td-compensation (Previous System). Car vibration is less than 5gal.

(2) Figure3.2: ω_c = 500rad/s, without H/W Td-compensation

(3) Figure3.3: ω_c = 2000rad/s, without H/W Td-compensation

(4) Figure3.4: ω_c = 5000rad/s, without H/W Td-compensation

The frequency required of the MCP to achieve comparable performance and vibration as the previous system (vibration<5gal), without H/W compensation, is a frequency response of 5000rad/s. To realize 5000rad/s, a stable current control calculation cycle of less than 50μs is required.

3.2.2 Program Loading/Data Transfer System of the MCP

During system initialization, the CC-CPU writes the MCP program data, reading from the flash memory, to the MCP program RAM directly. This is done to provide the flexibility of having the MCP program accessible for updates through the flash memory, while allowing high speed access to the program data through use of the AML internal RAM, which is much faster than external memory.

During MCP RUN mode (after initialization), the CC-CPU calculates the required torque and outputs the motor torque instruction to the MCP every 5ms. The MCP

updates the output to the converter/inverter with the new current command every 50μs. Even with such a different cycle speed, it is ensured that the data transfer between the CC-CPU and the MCP never disturbs or interrupts the other processor. This is done through the use of a high-speed asynchronous data buffer. It contains double registers each holding one data word, and synchronizes the data only while neither processor is accessing the register. Therefore, each processor is able to read/write with no wait state or interrupt.

A-D and D-A converters, PWM units for the inverter and the converter, and Encoder counters are also provided and connected directly to the MCP core. The inclusion of all these functional blocks has greatly reduced the part count of the controller as well as increasing reliability and performance.

3.2.3 The Original MCP Core

Taking advantage of the integration onto a single LSI chip, an original RISC logic core specialized to elevator driving was developed. Analyzing the actual motor control software, 48 16-bit fixed length instructions were provided. The Configuration of the MCP core is shown in figure 4. In addition to the RISC core a 32-bit fixed decimal point arithmetic logic unit (32bit+32bit, 16bit*16bit supported) was incorporated. Three stages (Load/Calculation/Store) are provided to enable pipelined operation. Each stage is able to operate in parallel, the calculation is proceeded with every clock cycle. With the development of the new MCP core, it was necessary to prepare an original assembler.

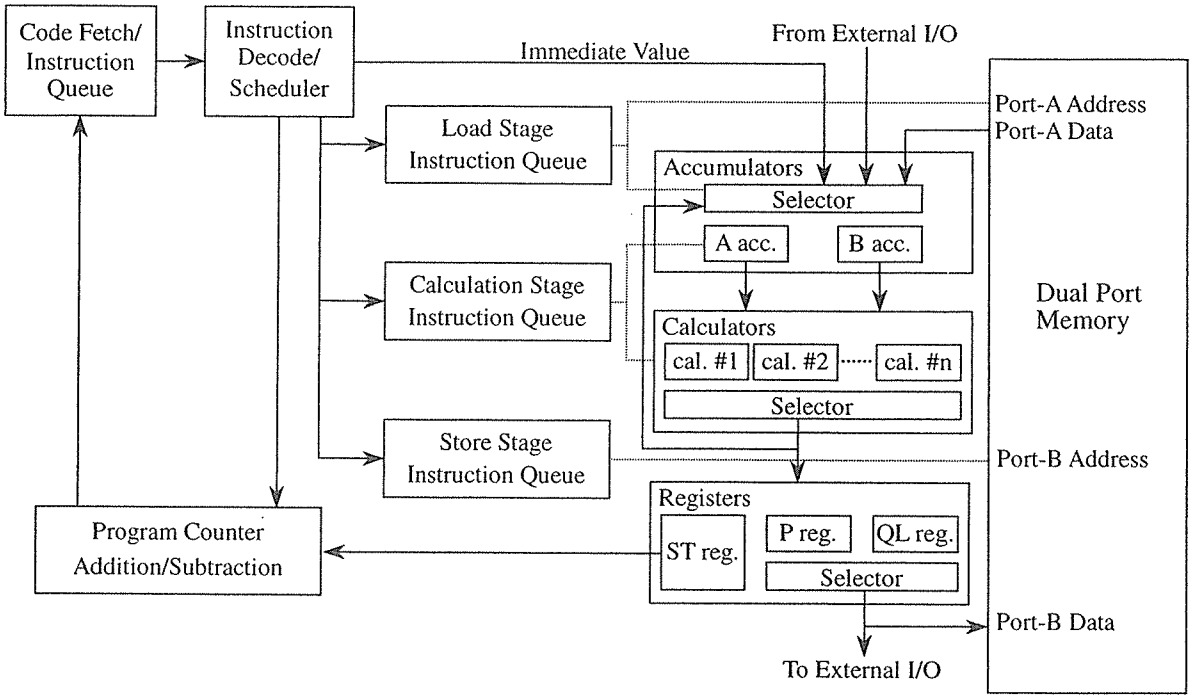


Figure4. Configuration of MCP Core

3.2.4 Debugging of the AML chip

The debugging flow diagram used for the AML chip is shown in Figure 5. An In-Circuit Emulator (ICE) was not able to be prepared as is generally done with processors. Instead, a "Virtual Debug" method was employed. In this method, an MCP emulator was prepared to generate a C-model of the AML chip. The C-model of the AML chip was generated using the MCP Emulator program. Matlab was used to link the above C-model of the MCP with the model of the converter/inverter unit and then simulate the complete motor control.

The MCP machine code compiled by the MCP assembler was loaded into the Virtual Prototyping System (Zuken-VPS, a product of Zuken Inc.) logic simulator which simulates the designed logic circuit. The Virtual debugging was performed by comparing the stored data on the registers of the C-model emulator with those on the Zuken-VPS simulator. Actual motor control functions were also confirmed through the Matlab simulation.

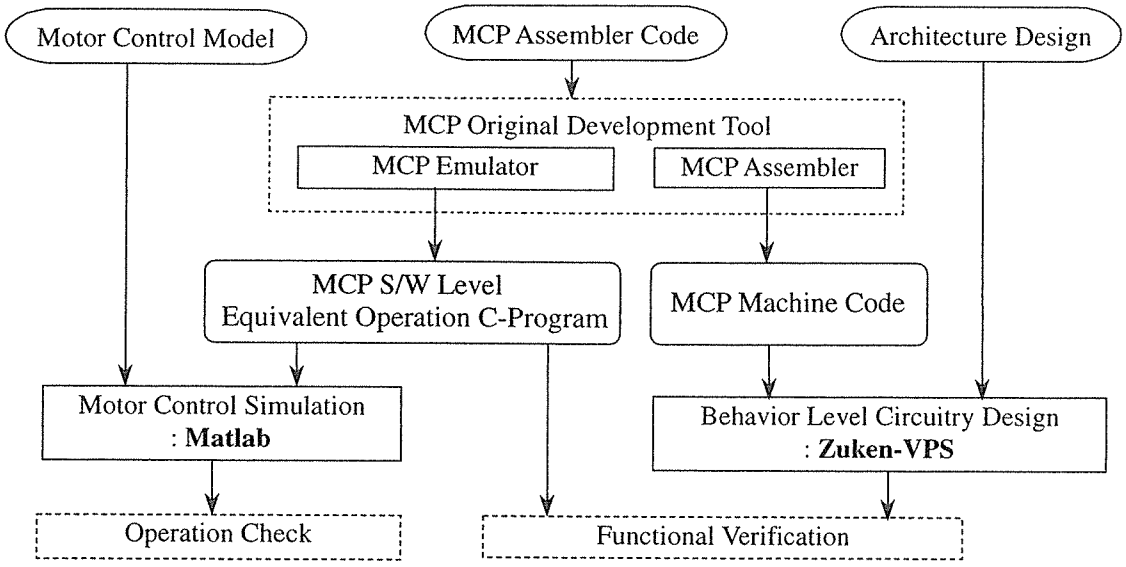


Figure 5. MCP Debugging Flow Diagram

4. ASIC Design and Verification Method of AML

4.1 Topdown design method

The design and verification process used in the development of the AML ASIC chip is shown in the design flow diagram of Figure 6. The best EDA tool available has been chosen for each functional circuit block. The development begins with a High-level circuit description in either Verilog-HDL(Hardware Description Language), or through the

use of Zuken-VPS functional blocks. The MCP core is described through Data flow diagram design entry. Zuken-VPS is used for design entry, functional simulation, and logic synthesis. For peripheral components, Verilog-HDL is used for the design entry. The components are described at a Register Transfer Level (RTL), and then this description is used for logic synthesis. Verilog-XL, a product of Cadence Design Systems Inc., is used for logic simulation, and Design Compiler, a product of Synopsys Inc., is used for logic synthesis. The output of the logic synthesis for both tools is a gate-level netlist mapped to the design library provided by the ASIC supplier.

Delay simulation is performed by the LSI vendor's tool. A Static timing analysis tool (Setup/Hold time analysis between flip-flops) is used to decrease the simulation time. Scan-pass design rules are employed to use ATPG(Auto Test Pattern Generator).

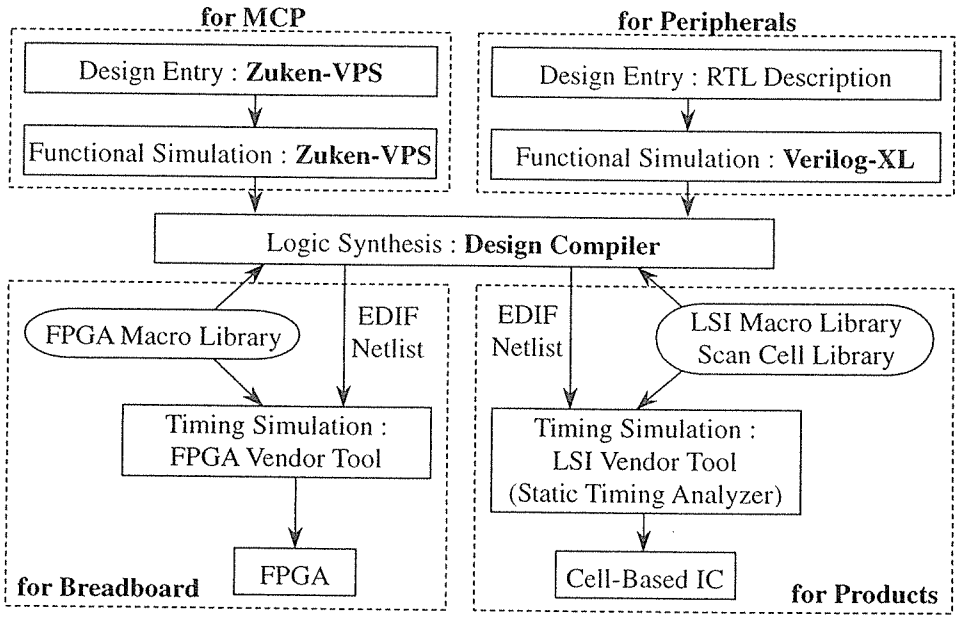
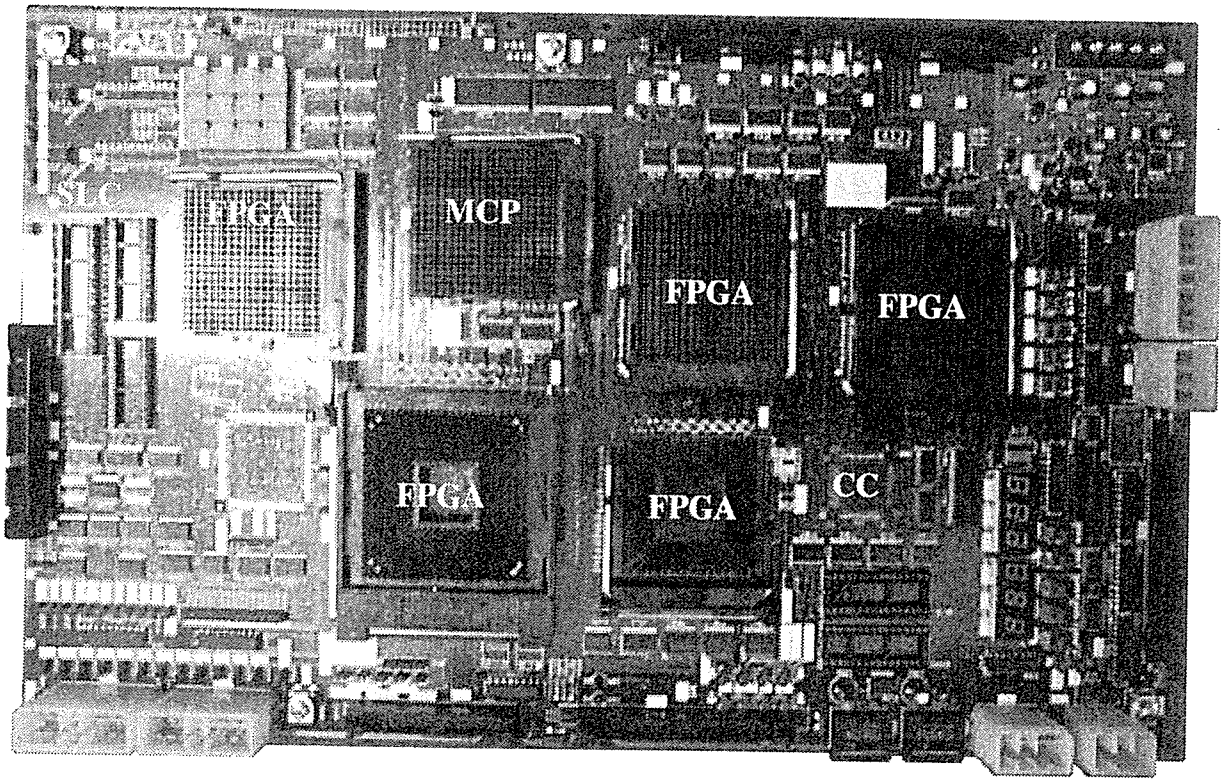


Figure 6. AML Design Flow Diagram

4.2 Verification by the breadboard

The breadboard for the actual elevator running test is shown in Figure 7. Functional blocks are emulated by one Gate Array and six FPGAs (Field Programmable Gate Array). For the H/W and S/W test of the MCP and user logic, an actual elevator car was run in the testing tower using this breadboard as the controller. By testing the breadboard, possibility of having to remake the ASIC after finalization of the design is minimized. Since the speed of the FPGA is limited, the clock speed had to be reduced to 25MHz. The normal AML base clock is 40MHz.



Board Size : 280mm by 450mm

Figure7. Breadboard for AML Verification

5. Conclusion

We completed the development of the above mentioned system LSI in 15 months. It took 5 months for determination of the functional specification, 2 months for HDL coding and functional simulation, 6 months for debugging by breadboard, and another 2 months for fitting to the target LSI and performing the delay simulation. Although this would not normally be enough time for a LSI of such a scale, we were able to obtain the final LSI without correcting the design after signoff.

We realized minimization of the control unit and cost reduction in this development. Moreover, we have proven this method effective for design and verification of system LSIs, even for those of a much larger scale.

Author Biographical Details:

Shigeki Yamakawa

Electrical Engineering Degree from Nagoya University in1984.
Joined Mitsubishi Electric Corporation in1984.
Presently Assistant Manager of Elevator Electrical Development Section of Inazawa Works, Mitsubishi Electric Corporation, Japan.

Hiroshi Gokan

Engineering Degree of Mathematical Sciences from University of Osaka Prefecture in 1987.
Joined Mitsubishi Electric Corporation in 1987.
Presently Assistant Manager of Electronic Design Engineering Dept. of Design Systems Engineering Center, Mitsubishi Electric Corporation, Japan.

Hiroshi Araki

Electrical Engineering Degree from Shizuoka University in1985.
Joined Mitsubishi Electric Corporation in1985.
Presently Assistant Manager of Elevator Electrical Development Section of Inazawa Works, Mitsubishi Electric Corporation, Japan.

Hiroyuki Ikejima

Electrical Engineering Master's Degree from Kobe University in1980.
Joined Mitsubishi Electric Corporation in1980.
Presently Manager of Elevator Electrical Development Section of Inazawa Works, Mitsubishi Electric Corporation, Japan.