NEW TECHNOLOGIES FOR ELEVATOR CONTROL SYSTEM

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ABSTRACT

This paper describes the control system applied to Mitsubishi Electric Corporation's newly developed GPS-II Series elevators. The latest electronics and computer technologies incorporated into this next generation of variable-voltage variable-frequency (VVVF) control system are discussed.

1 INTRODUCTION

More than a decade has passed since the Corporation developed the first VVVF controlled elevator in 1983. In these ten years there has been great progress in the area of electronics and computer engineering. Making good use of the latest electronics and computer technologies, the Corporation began marketing the standardized GPS-II Series elevators October 1995.

Table 1 shows the history of Mitsubishi VVVF controlled standard type elevators. The GPS-II Series is the third generation of the VVVF control. The control system of the GPS-II Series is based on that of the previous GPS Series, but the system has been significantly upgraded by incorporating high-performance microprocessors and newly developed application-specific integrated-circuits, or ASICs.

Table 1 History of Mitsubishi VVVF Controlled Standard Type Elevators

Elevator Series	SP-VL	GPS	GPS-II
Rated Capacity in kg	450 to 1,000	450 to 1,000	450 to 1,350
Rated Speed in m/min	45 to 105	45 to 105	45 to 150
Control System	Centralized Processing	Distributed Processing	Distributed Processing
Car Control	8-Bit MPU	16-Bit MPU	32-Bit MPU, ASIC
Motion Control	Analogue PWM	Analogue PWM	Digital PWM, ASIC
Converter Module	Diode	Diode	Diode
Inverter Module	PTR	IGBT	IPM, IGBT
First Product	1985	1992	1995

[Notes] ASIC: Application-Specific Integrated-Circuit
IGBT: Insulated-Gate Bipolar-Transistor
IPM: Intelligent Power-Module
MPU: Microprocessing Unit
PTR: Power Transistor
PWM: Pulse-Width Modulation

Features of the GPS-II Series include:

◇ the capacity and speed range increased to 1,350kg and 150m/min respectively, cf. those of the previous series at 1,000kg and 105m/min;

◇ a network-based elevator control system consisting of multiple microprocessors distributed to a machine room, an elevator car, and each hall;

◇ a control panel provided with a 32-bit microprocessor and dedicated ASICs;

◇ an all digital motion control system incorporating digitized pulse-width modulation (PWM) circuit; and

◇ a VVVF inverter unit consisting of a diode module, electrolytic capacitors, an intelligent power-module or IPM, and current sensors all of which are mounted on a printed-circuit board in order to eliminate bus bars or electric wires.

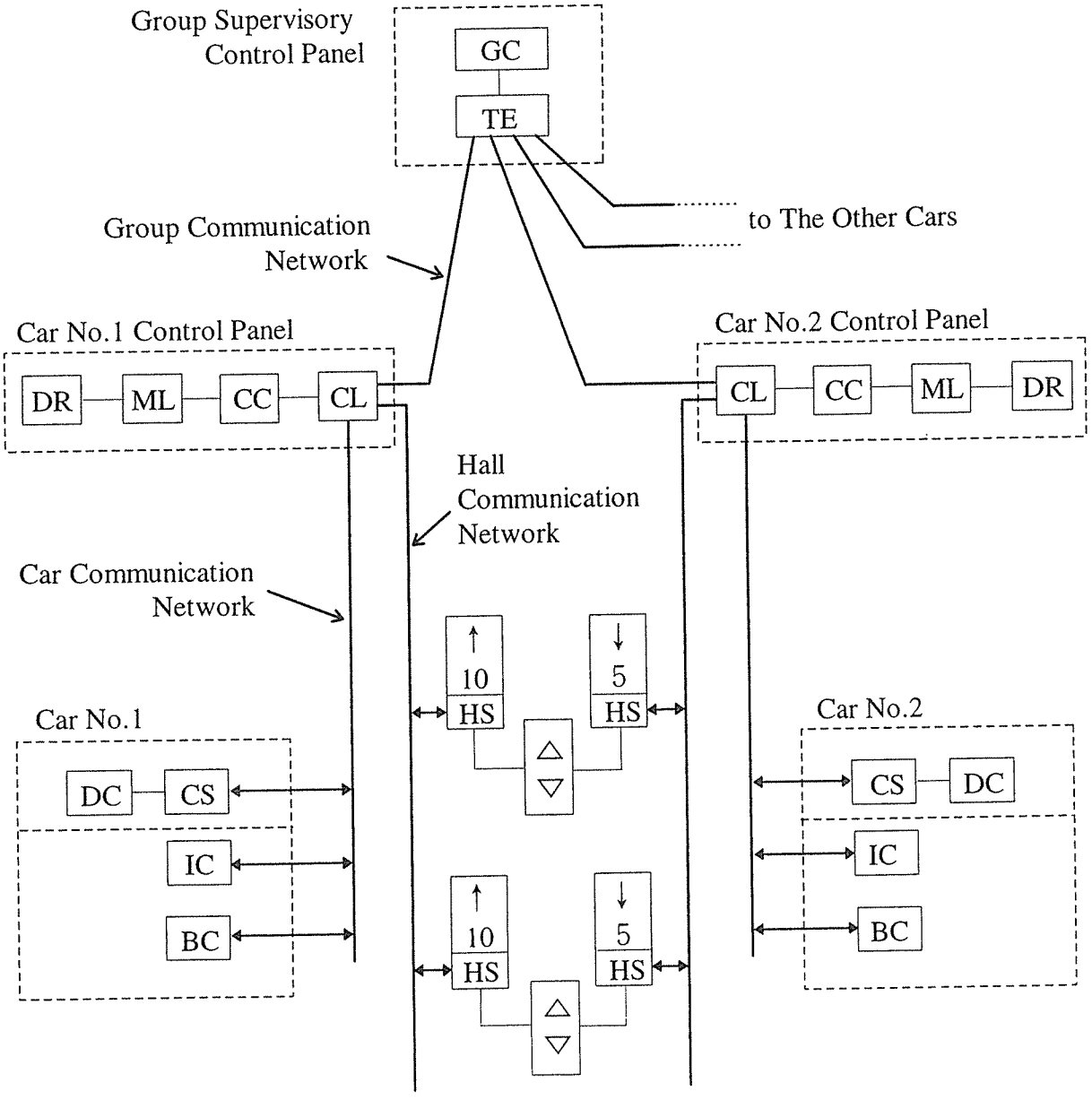

Figure 1 Overall Configuration of GPS-II Elevator Control System

Table 2 Microprocessors and Application-Specific Integrated-Circuits

Name	Description
GC	16-bit Microprocessor for Group Supervisory Control
TE	8-bit Microprocessor for Serial Communication
CC	32-bit Microprocessor for Car Operation Controller and Motion Controller
CL	Application-Specific Integrated-Circuit (ASIC), Incorporating 8-bit Microprocessor and approx. 110,000 Gates
DR	16-bit Microprocessor for Motion Controller
ML	Application-Specific Integrated-Circuit, Incorporating approx. 60,000 Gates
CS	8-bit Microprocessor for Serial Communication
DC	16-bit Microprocessor for Door Operator
IC	8-bit Microprocessor for Car-Position Indicator
BC	8-bit Microprocessor for Car Operating Panel
HS	8-bit Microprocessor for Hall Signal Fixtures

2 ELEVATOR CONTROL SYSTEM

2.1 System Configuration

Figure 1 illustrates an overall configuration of the elevator control system for the GPS-II Series. Table 2 lists the microprocessors and ASICs incorporated into the system. The elevator control system comprises a number of microprocessors distributed to a machine room, an elevator car, and each hall. These microprocessors are interconnected by three independent serial communication networks, a group communication network, a car communication network, and a hall communication network.

A group supervisory control panel is equipped with two microprocessors, GC and TE. The GC implements group supervisory control. The TE forms the group communication network to handle serial communication with each car control panel. An optical-fiber cable is used for the group communication network.

A control panel is equipped with two microprocessors, CC and DR; and two dedicated ASICs, CL and ML. The functions of these microprocessors and ASICs are described in more depth later in the paper.

Two microprocessors, CS and DC, are mounted on top of the car. The CS forms the car communication network to receive and transmit signals between the control panel and the car. The DC is engaged in the door drive system which is also VVVF controlled.

Inside the car are two microprocessors, IC and BC. The IC and BC communicate with the control panel to control the car-position indicator and the car operating panel respectively.

Each hall is also provided with microprocessor(s), HS. The HS forms the hall communication network to control the hall call buttons and the car-position indicator or the direction lantern.

2.2 Car Control System

Each car control system comprises three major portions, a car operation controller, a motion

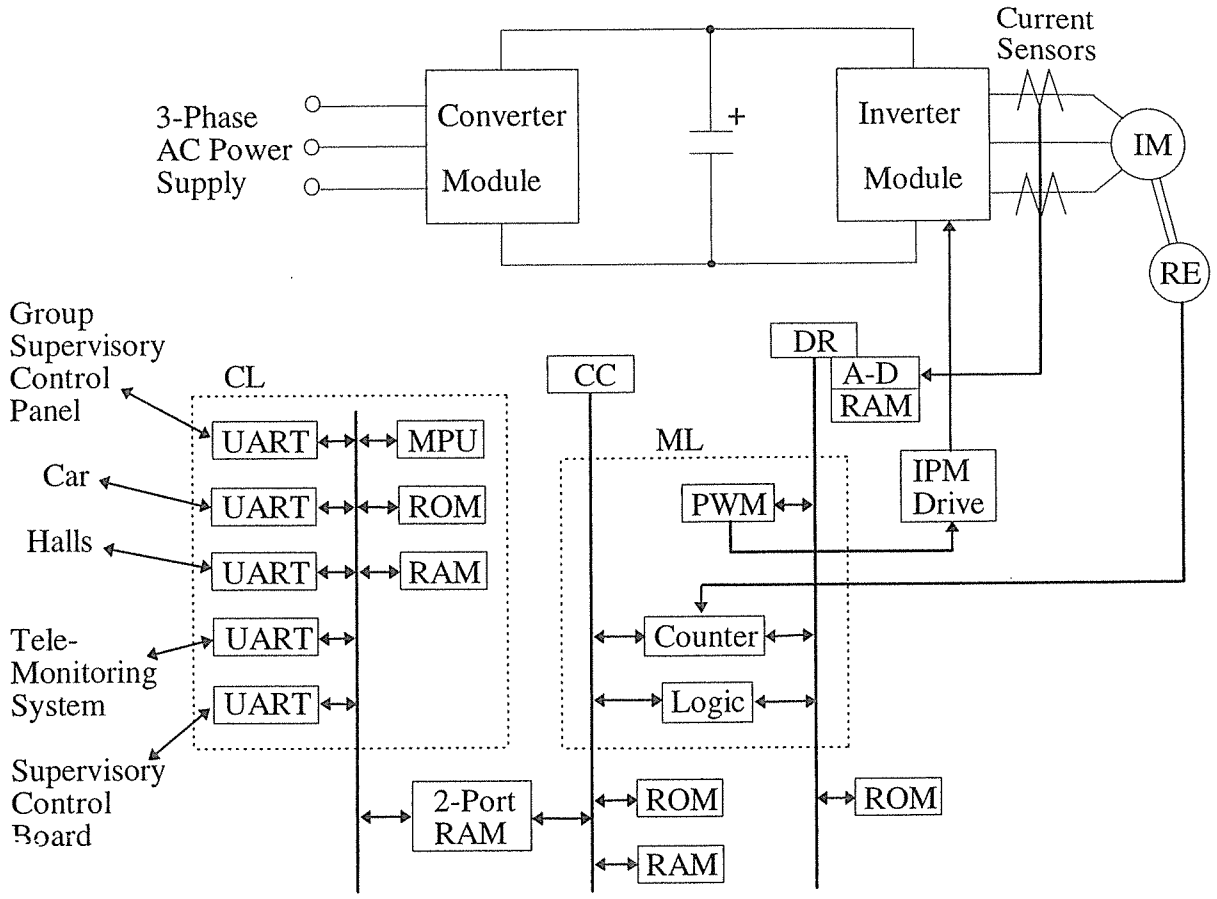

Figure 2 Block Diagram of Control Panel

controller, and a motor controller. Details of each controller are described below.

2.2.1 Car Operation Controller

Figure 2 is a block diagram of the control panel. The car operation controller consists of the CC and CL. The CC is a 32-bit microprocessor that runs at 14.7456 megahertz. The CL is the said ASIC newly developed exclusively for the GPS-II Series and incorporates an 8-bit microprocessor which is described as MPU in Figure 2, read-only memories or ROMs, random-access memories or RAMs, and universal asynchronous receiver transmitters or UARTs. The CL contains approximately 110,000 gates and the package of the CL is a surface-mounting type having 120 pins.

The CC implements car call assignment and door control. The CL receives and transmits signals between the control panel and the group supervisory control panel, between the control panel and the car, and between the control panel and the halls. The CL also has UARTs for communicating with optional equipment, such as a tele-monitoring system and a supervisory control board. Signal transmission between the CC and the CL is handled by a 2-port random-access memory or 2-port RAM.

2.2.2 Motion Controller

The motion controller consists of the CC, DR, and ML. The CC is the aforementioned 32-bit microprocessor. The DR is a general purpose 16-bit microprocessor having an analogue-to-digital (A-D) converter and a random-access memory or RAM. The ML is the forenamed ASIC developed exclusively for the GPS-II Series, which includes a digital pulse-width modulation (PWM) circuit, a counter for counting rotary-encoder (RE) pulses, and a logic circuit for signal transmission between the CC and DR, as shown in Figure 2. The ML contains approximately 60,000 gates and the package of the ML is a surface-mounting type having 304 pins.

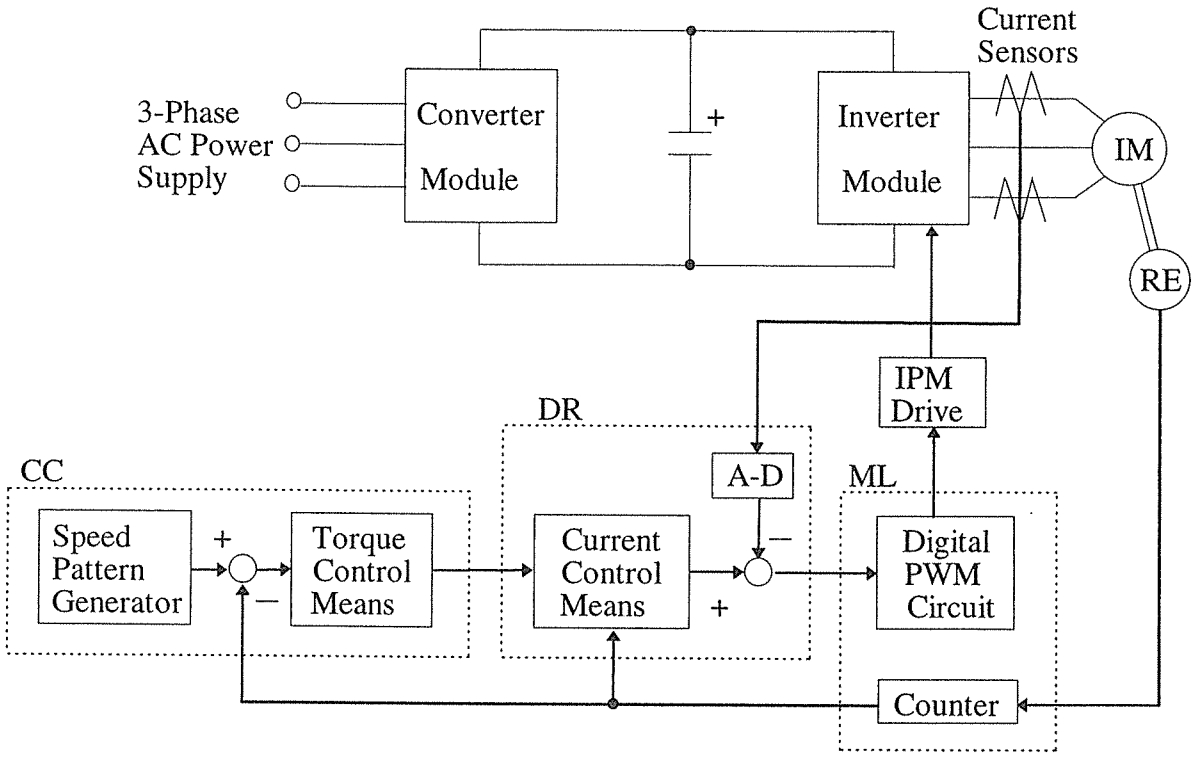

Figure 3 Block Diagram of Motion Controller

Figure 3 is a block diagram of the motion controller. The CC has also been utilized for the motion controller, since the CC is a high-performance 32-bit microprocessor whose speed of executing programs is high enough to perform the motion control as well as the car operation control.

The CC functions as:

a speed pattern generator which generates a speed instruction of the car;

a comparator which calculates an error between the said speed instruction and speed-feedback signal from the counter; and

a torque control means which creates the motor torque instruction.

The A-D converter incorporated into the DR converts analogue motor currents detected by current sensors into digital values.

The DR functions as:

a current control means which, every 500 microseconds, calculates motor current instructions from the said motor torque instruction and the speed-feedback signal; and

a comparator which, every 500 microseconds, calculates motor voltage instructions by comparing the said motor current instructions with the motor currents digitized by the A-D converter.

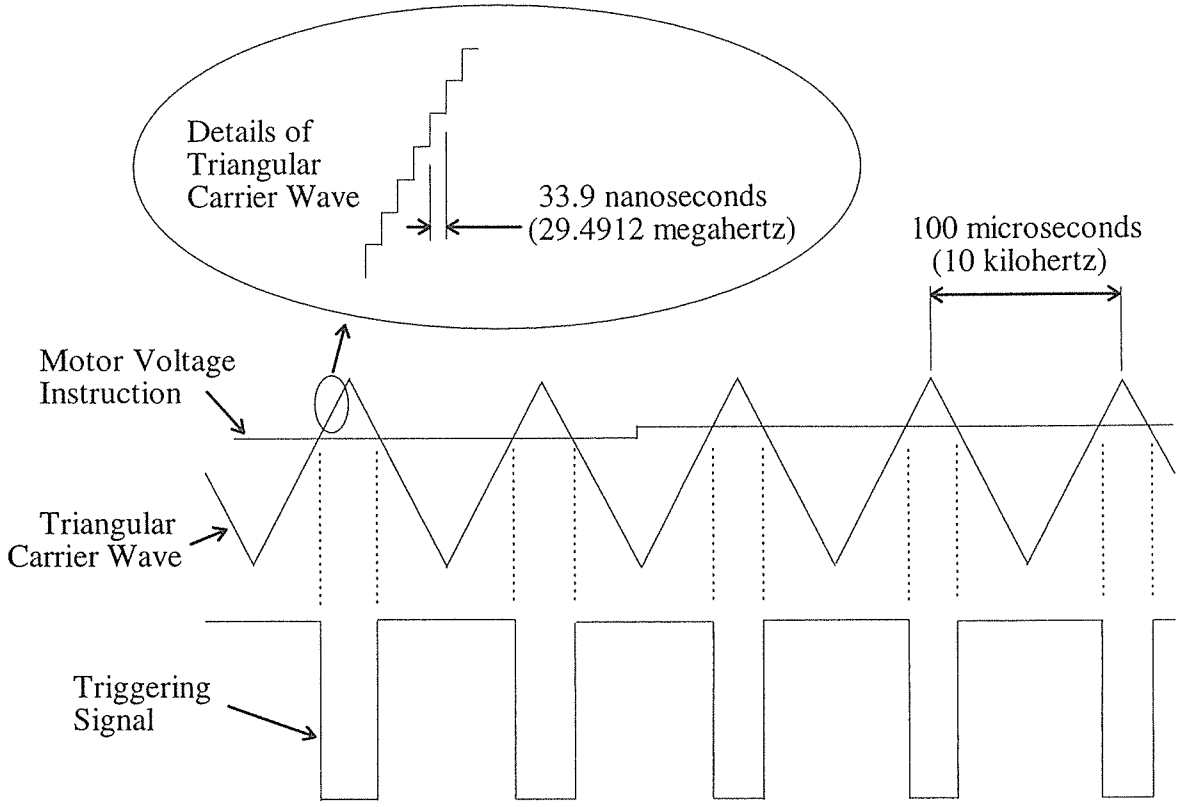

Figure 4 Digital Pulse-Width Modulation

Figure 4 illustrates waveforms generated by the digital PWM circuit. A master clock of the PWM circuit is 29.4912 megahertz.

The digital PWM circuit consists of:

a 12-bit up-down counter which counts the master clock to create a 10-kilohertz triangular carrier wave; and

a comparator which compares the aforementioned motor voltage instructions with the triangular carrier wave to provide triggering signals of the intelligent power-module (IPM) every approximately 33.9 nanoseconds, that is, the reciprocal of 29.4912 megahertz.

Thus the resolution of the triangular carrier wave is:

$$(29.4912 \text{ megahertz}) / (10\text{-kilohertz}) / 2 = 1475$$

The master clock of 29.4912 megahertz and the resolution of the triangular carrier wave of 1475, have been carefully selected in order to make motor voltage approximate a sinusoidal wave.

2.2.3 Motor Controller

The VVVF inverter has been adopted as a motor controller for the GPS-II Series as well as the previous series. Recently, the intelligent power-module (IPM) has begun taking the place of insulated-gate bipolar-transistor (IGBT) module because the IPM contains not only an IGBT module but also an IGBT drive circuit and protection circuits, such as short circuit, over-current, overheat, under-voltage of power supply, etc. For the GPS-II Series, IPMs with the rated current of 75 and 150 amperes have been utilized. These effectively cover the capacity and speed range up to 1000kg-45m/min or 900kg-60m/min. As to the capacity and speed range beyond the IPM application, IGBT modules are still used.

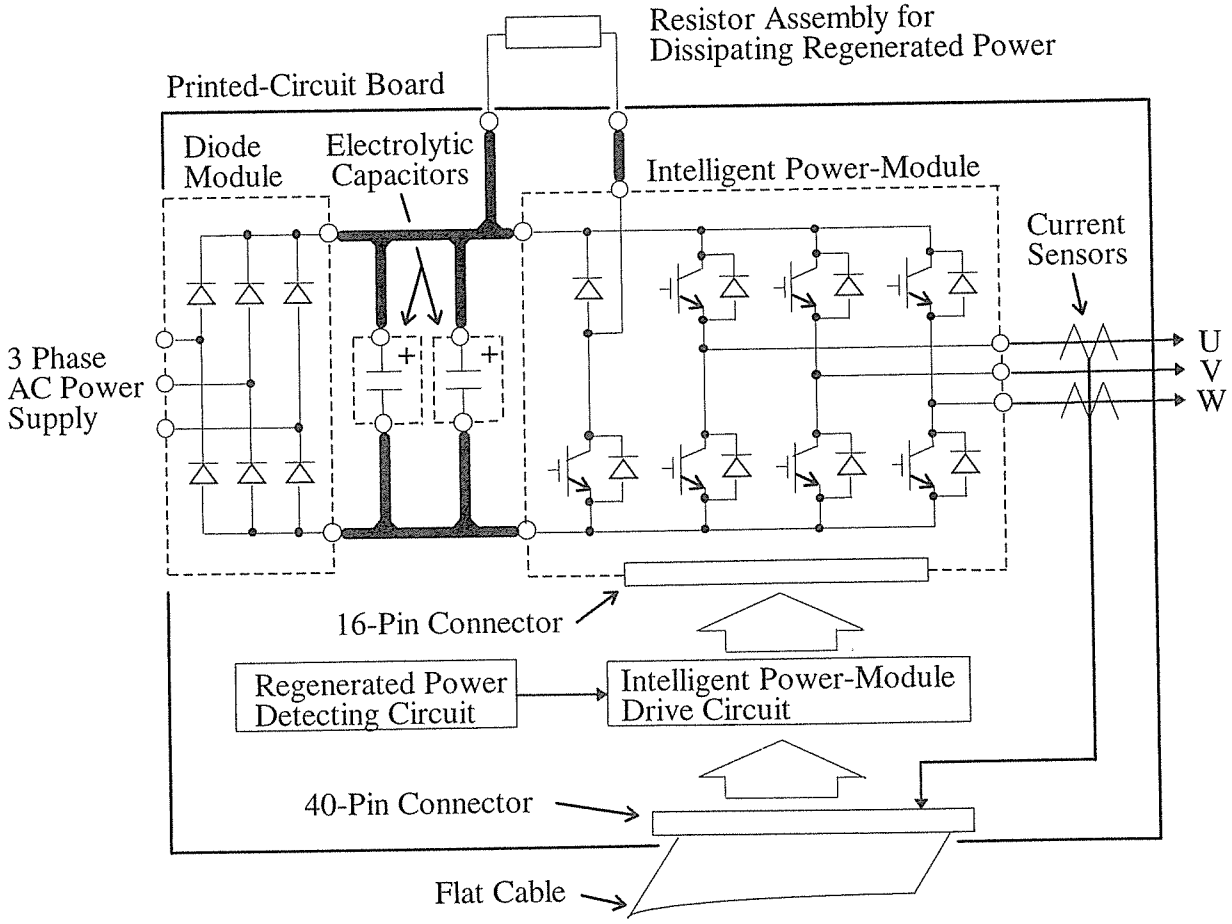

Figure 5 Block Diagram of VVVF Inverter Unit

Figure 5 illustrates a block diagram of a VVVF inverter unit incorporating the IPM. 3-phase AC power supply is rectified to DC by a diode module, smoothed by electrolytic capacitors, and then reconverted into 3-phase AC by the IPM. A resistor assembly for dissipating regenerated power consumes regenerated power from a hoisting motor when detected by a regenerated power detecting circuit. The aforementioned triggering signals created by the digital PWM circuit are fed to the IPM drive circuit through a flat cable with 40-pin connectors. The IPM drive circuit consists of photo-couplers to isolate the triggering signals from each element of the IPM.

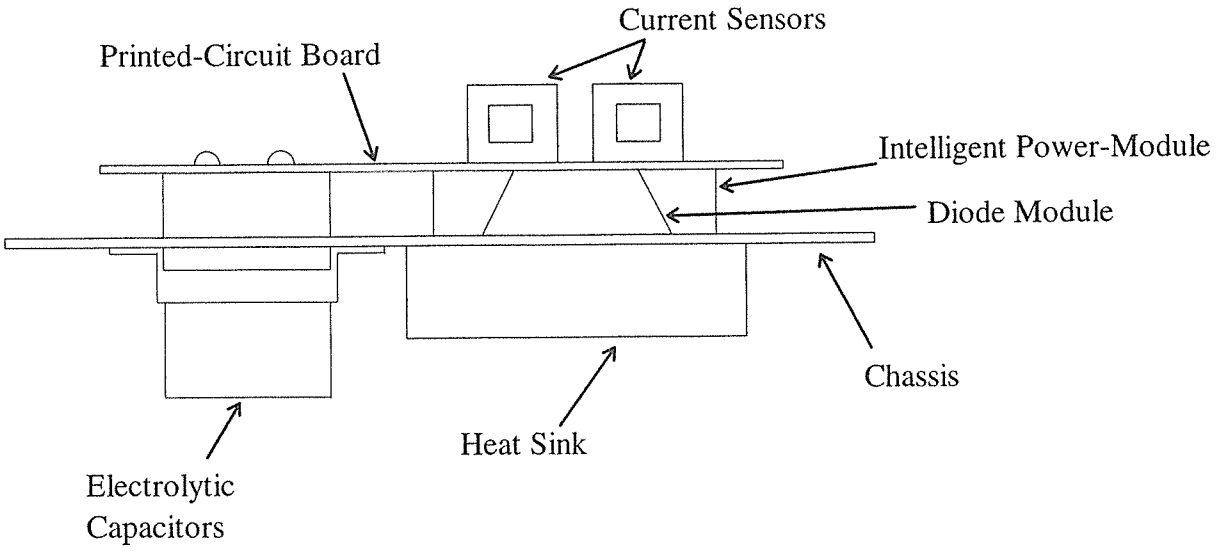

Figure 6 Assembly of VVVF Inverter Unit

Bus bars or electric wires have commonly been used for connecting large-current components or modules. But for the GPS-II Series a printed-circuit board has been utilized in lieu of the bus bars and electric wires.

Figure 6 shows an assembly of the VVVF inverter unit incorporating the IPM.

The VVVF inverter unit comprises:

a heat sink onto which the diode module and the IPM are mounted, the diode module and the IPM having the same height;

a chassis having a rectangular hole to fix the heat sink with the diode module and the IPM, and two round holes to fix two electrolytic capacitors;

two electrolytic capacitors fixed to the chassis so that their terminals align with the diode module and the IPM in height;

a printed-circuit board on which are mounted two current sensors, an IPM drive circuit, the regenerated power detecting circuit, a 16-pin connector, a 40-pin connector, etc.;

the said printed-circuit board secured by screws to two output terminals of the diode module, four terminals of the electrolytic capacitors, two input terminals of the IPM, and a terminal of the IPM for dissipating the regenerated power.

The 3-phase AC power supply is directly connected to the input terminals of the diode module. Two wires for the hoisting motor are passed through the current sensors and connected to two of the three output terminals of the IPM, while a remaining wire is directly connected to one of the three output terminal of the IPM.

Copper-pattern thickness of the printed-circuit board is 105 microns for a 75-ampere IPM, and 175 microns for a 150-ampere IPM. The copper-patterns are remarkably thick when compared to the 18 microns for regular printed-circuit boards.

3 CONCLUSION

The GPS-II Series elevators incorporates the latest electronics and computer technologies and has the following advantages:

◇ The number of printed-circuit boards has been reduced by the adoption of the 32-bit microprocessor and the ASICs.

◇ Excellent ride performance has been obtained by means of the high-resolution digital control system.

◇ Adjustment-free and maintenance-free motion control has been achieved by means of the high-resolution digital control system.

◇ Assembly of the VVVF inverter unit has been greatly simplified by the use of the printed-circuit board in place of bus bars or electric wires for connecting inverter components.

The introduction of VVVF inverters and microprocessors has played a major role in the advancement of elevators. The Corporation continues integrating the advanced technologies into today's elevators in an effort to meet customers' needs with higher performance and safety, and providing more sophisticated functions.

BIOGRAPHY

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